AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. – 19. (Cancelled)

20. (Currently Amended) A wiring tape for a semiconductor device, which comprises a wiring layer comprising an insulating layer and a wiring on the insulating layer, one end of the wiring being connected to terminals on a semiconductor chip and the other end of the wiring being connected to external terminals for connecting to a package substrate; and a three-layered buffer elastomer layer bonded to a wiring-formed side of the wiring layer, the buffer elastomer layer comprising a structure having interconnected foams or a three-dimensional reticular structure, an adhesive layer provided on the semiconductor chip-facing side of the structure having interconnected foams or the three-dimensional reticular structure, ~~directed~~ to ~~bonding~~ bond to the semiconductor chip and another adhesive layer provided on the other side of the structure, ~~directed~~ to ~~bonding~~ bond to the wiring-formed side of the wiring layer to relax thermal stress generated between the semiconductor chip and the package substrate during heating.

21. (Previously Presented) A wiring tape according to Claim 20, wherein a thickness ratio of the structure having interconnected foams or the three-dimensional reticular structure to total buffer layer thickness is at least 0.2 to reduce the likelihood

of failure of the semiconductor device during heating performed in a reflow operation used in manufacturing the semiconductor device.

22. (Previously Presented) A wiring tape according to Claim 20, wherein the buffer layer is comprised of a laminate prepared by pasting both sides of the structure having interconnected foams or the three-dimensional reticular structure with the adhesive layers, respectively.

23. (Original) A wiring tape according to Claim 20, wherein the buffer layer is composed of a laminate prepared by pasting both sides of the structure having interconnected foams with adhesive layers each comprising a structure having interconnected foams whose pores are filled with an adhesive, respectively.

24. (Currently Amended) A wiring tape for a semiconductor device, which comprises a wiring layer comprising an insulating layer and a wiring on the insulating layer, one end of the wiring being connected to terminals on a semiconductor chip and the other end of the wiring being connected to external terminals for connecting to a package substrate; and means for relaxing thermal stress generated between the semiconductor chip and the package substrate and for releasing steam pressure generated during heating in a reflow operation used in forming a package, including the wiring tape and the semiconductor device, to outside of the package, said means comprising:

a three-layered buffer elastomer layer bonded to a wiring-formed side of the wiring layer, the buffer elastomer layer comprising a structure having interconnected

foams or a three-dimensional reticular structure, an adhesive layer provided on the semiconductor chip-facing side of the structure having interconnected foams or the three-dimensional reticular structure, ~~directed to bonding~~ to bond to the semiconductor chip and another adhesive layer provided on the other side of the structure, ~~directed to bonding~~ bond to the wiring-formed side of the wiring layer.

25. (Currently Amended) A wiring tape according to Claim 24, wherein a thickness ratio of the structure having interconnected foams ~~of~~ or the three-dimensional reticular structure to total buffer layer thickness is at least 0.2 to reduce the likelihood of failure of the semiconductor device during heating performed in a reflow operation used in manufacturing the semiconductor device.

26. (Previously Presented) A wiring tape according to Claim 24, wherein the buffer layer is comprised of a laminate prepared by pasting both sides of the structure having interconnected foams or the three-dimensional reticular structure with the adhesive layers, respectively.

27. (New) A wiring tape according to Claim 20, wherein the adhesive layer on the semiconductor chip-facing side is directly bonded to the semiconductor chip and the other adhesive layer is directly bonded to the wiring-formed side of the wiring layer.

28. (New) A wiring tape according to Claim 24, wherein the adhesive layer on the semiconductor chip-facing side is directly bonded to the semiconductor chip

and the other adhesive layer is directly bonded to the wiring-formed side of the wiring layer.